HT4168 Transmission IC for RFID read only

Summary

HT4168 is the RFID read transmission circuit that is formed by CMOS. The electronic power is provided by the electronic coil of HT4168's 2 pins, and the operation pulse is provided through the same path. HT4168's application is to adjust radio frequency to make 64 bits data loading on RF. This is the reason that HT4168 can transfer data by RFID.
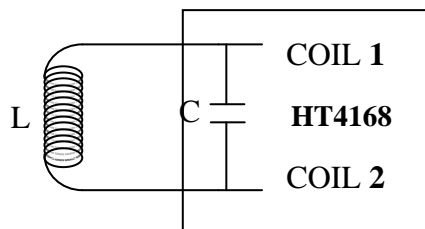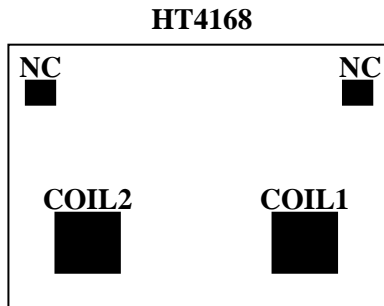
Outside circuit

Fig.(一)
IC capacitor 470pF

HT4168's pin Assignment

COIL1 / CLOCK INPUT
COIL2 / DATA TRANSMISSION
PAD size 106um*106um
Chip size 698um×595um
Fig.(二)

Electronic condition

Table (一)

Parameter	Min	Typical	Max	Unit
operation temperature	-40		+85	℃
operation voltage	3.5	5		V
operation frequency	100		150	MHz
storage temperature	-55		+200	℃
ESD capability		2000		V

Code Format

The binary code	0	1	1	0	1	0	0	1

Output before adjustment

Output after adjustment

Fig.(三)

TIMING

T_{oc} 64 T_{oc}

COIL 1

SERIAL DATA   **Bit**   **Bit n+1**   **Bit n+2**

Fig.(四)

IC BLOCK

Timing generation

Coil1

Clock

AC1 Full-wave rectification

Sort

Memory array

AC2

Coil2

data adjustment

Data out

data coding
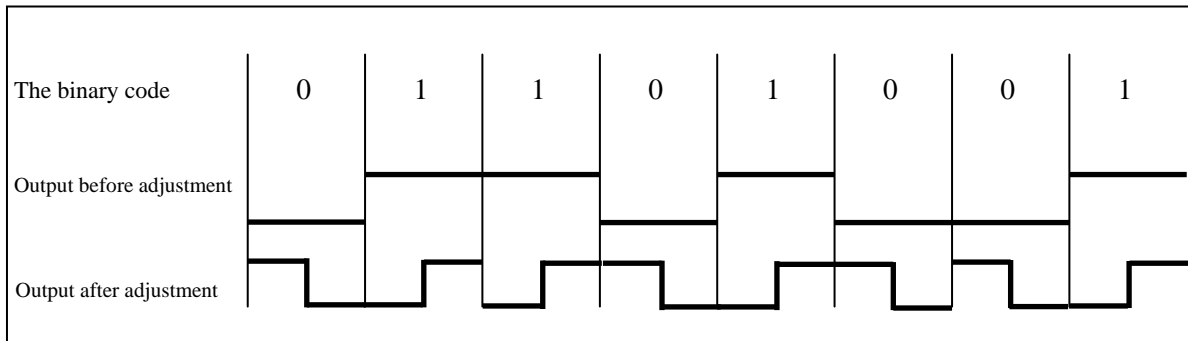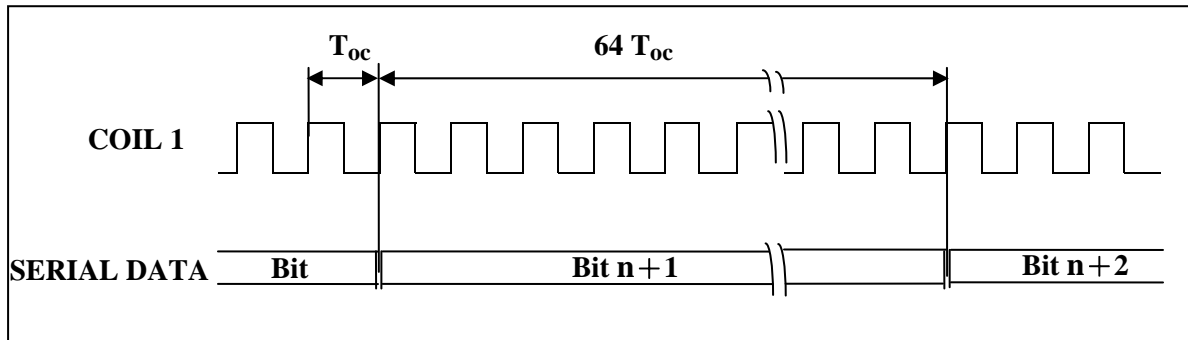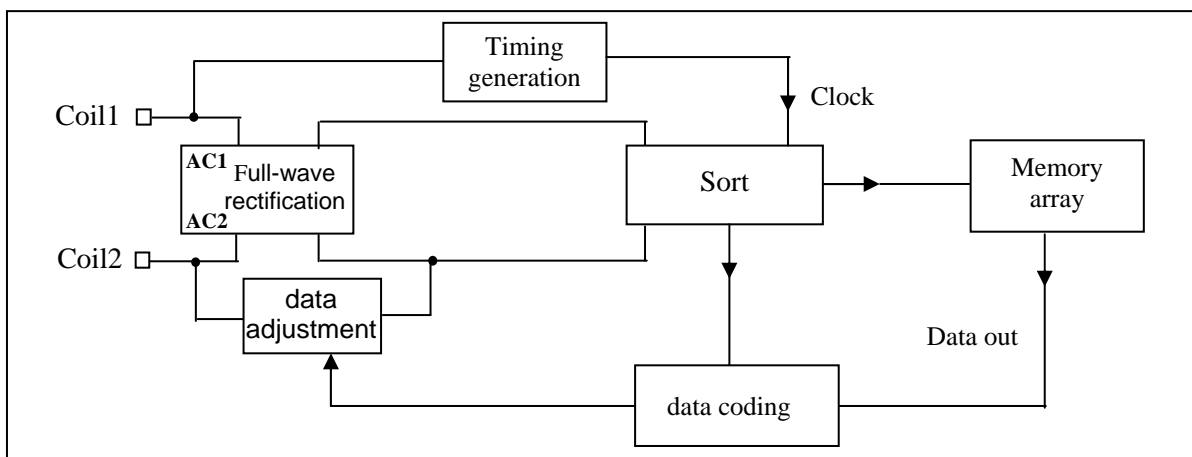
Fig.(五)

MEMORY ARRAY

   THE HT4168 CONTAINS 64 BITS DIVIDED IN FIVE GROUPS OF INFORMATION. 9 BITS
ARE USED FOR THE HEADER, 10 ROW PARITY BITS (P0-P9), 4 COLUMN PARITY BITS
(PC0-PC3), 40 DATA BITS (D00-D93), AND 1 STOP BIT SET TO LOGIC 0.

1	1	1	1		1	1	1	1		1	- 9 BITS HEADER
8 VERSION BITS OR					**D00 D01 D02 D03**					**P0**	- 4 DATA BITS AND
CUSTOMER ID					**D10 D11 D12 D13**					**P1**	ASSOCIATED EVEN ROW PARIY
					D20 D21 D22 D23					**P2**	BIT
					D30 D31 D32 D33					**P3**	
32 DATA BITS					**D40 D41 D42 D43**					**P4**	
ALLOWING 4 BILLION					**D50 D51 D52 D53**					**P5**	
OF COMBINATIONS					**D60 D61 D62 D63**					**P6**	
					D70 D71 D72 D73					**P7**	
					D80 D81 D82 D83					**P8**	- 4 COLUMN EVEN PARITY BITS,
					D90 D91 D92 D93					**P9**	NO ROW PARITY BIT
					PC0 PC1 PC2 PC3					**0**	

   THE HEADER IS COMPOSED BY THE 9 FIRST BITS WHICH ARE MASK PROGRAMMED
TO 1 1 1 1 1 1 1 1 1. DUE TO THE DATA AND PARITY ORGANISATION, THIS SEQUENCE
CANNOT BE REPRODUCED IN THE DATA STRING. THE HEADER IS FOLLOWED BY 10
GROUPS OF 4 DATA BITS AND 1 EVEN ROW PARITY BIT. THEN, THE LAST GROUP
CONSISTS OF 4 EVEN COLUMN PARITY BITS WITHOUT ROW PARITY BIT. BITS D00 TO
D03 AND BITS D10 TO D13 ARE CUSTOMER SPECIFIC IDENTIFICATION.
   THESE 64 BITS ARE OUTPUTTED SERIALLY IN ORDER TO CONTROL THE
MODULATOR USED TO MODIFY THE CURRENT AT ONE OF THE COIL TERMINALS.
WHEN THE 64 BITS DATA STRING IS OUTPUTTED, THE OUTPUT SEQUENCE IS
REPEATED CONTINUOUSLY UNTIL POWER GOES OFF.

CHIP DIMENSIONS

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