# HT4192 Read Only Contact Identification Device

## FEATURES

※ The HT4192 is compatible with the DS1990 Extended 2.8 to 5.25 voltage range
※ Unique, 64-bit registration number (8-bit family code + 48 bit serial number + 8-bit CRC tester);guaranteed no two parts alike
※ 8-bit family code specifies HT4192 communications requirements to reader
※ Presence Pulse acknowledges when the reader first applies voltage
※ Reduces control, address, data, and power to a single pin
※ Zero standby power required
※ Directly connects to a single port pin of a microprocessor and communicates at up to 16.3kbits/s
※ Applications
  ＊ PCB Identification
  ＊ Network Node ID
  ＊ Equipment Registration
※ Operates over industrial temperature range of -40°C to +85°C

## DESCRIPTION

The HT4192 enhanced Silicon Serial Number is a low-cost, electronic registration number that Provides an absolutely unique identity which can be determined with a minimal electronic interface (typically, a single port pin of a microcontroller). The HT4192 consists of a factory-lasered, 64-bit ROM that includes a unique 48-bit serial number, an 8-bit CRC, and an 8-bit Family Code (01h). Data is transferred serially via the HT-Wire protocol that requires only a single data lead and a ground return. Power for reading and writing the device is derived from the data line itself with no need for an external power source.

## OPERATION

The HT4192's internal ROM is accessed via a single data line. The 48-bit serial number, 8-bit family code and 8-bit CRC are retrieved using the HT-Wire protocol. This protocol defines bus transactions in terms of the bus state during specified time slots that are initiated on the falling edge of sync pulses from the bus master. All data is read and written least significant bit first.

## HT-Wire BUS SYSTEM

The HT-Wire bus is a system which has a single bus master system and one or more slaves. In all instances, the HT4192 is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and HT-Wire signaling (signal type and timing).

## Hardware Configuration

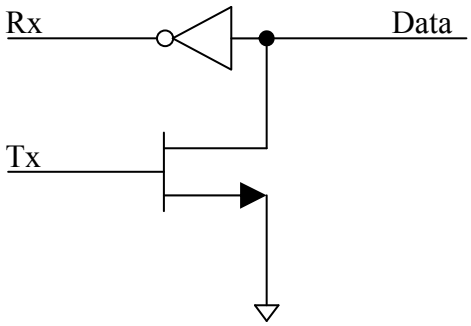
The HT-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the HT-Wire bus must have an open-drain connection or 3-state outputs. The HT4192 is an open-drain part with an internal circuit equivalent to that shown in Figure 2. The bus master can be the same equivalent circuit. If a bidirectional pin is not available, separate output and input pins can be tied together. The bus master requires a pullup resistor at the master end of the bus, with the bus master circuit equivalent to the one shown in Figure 3.

The value of the pullup resistor should be approximately 5kΩ for short line lengths. A multidrop bus consists of a HT-Wire bus with multiple slaves attached. The HT-Wire bus has a maximum data rate of 16.3kbits per second.The idle state for the HT-Wire bus is high. If, for any reason, a transaction needs to be suspended, the busMUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left lowfor more than 120 μs, one or more of the devices on the bus may be reset.

## HT4192 MEMORY MAP Figure 1

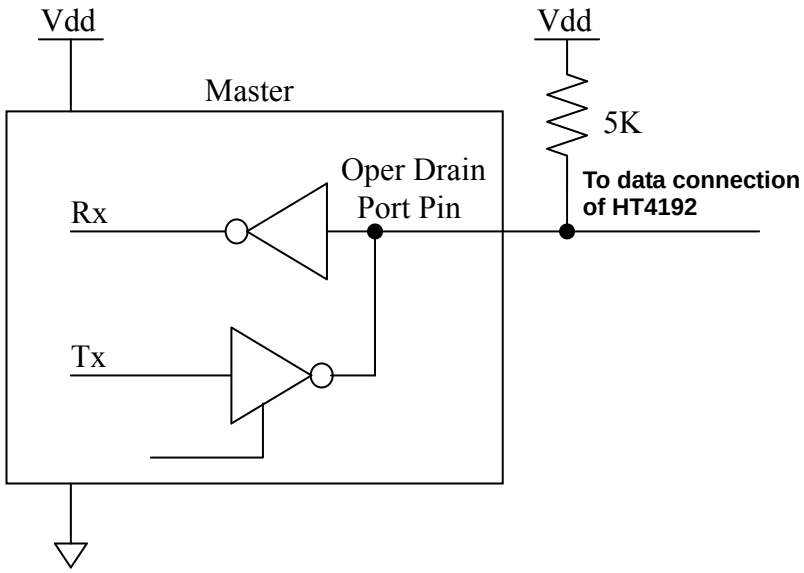
| 8-Bit CRC Code | | 48-Bit Serial Number | | 8-Bit Family Code (01h) | |
|---|---|---|---|---|---|
| MSB | LSB | MSB | LSB | MSB | LSB |

## HT4192 EQUIVALENT CIRCUIT Figure 2

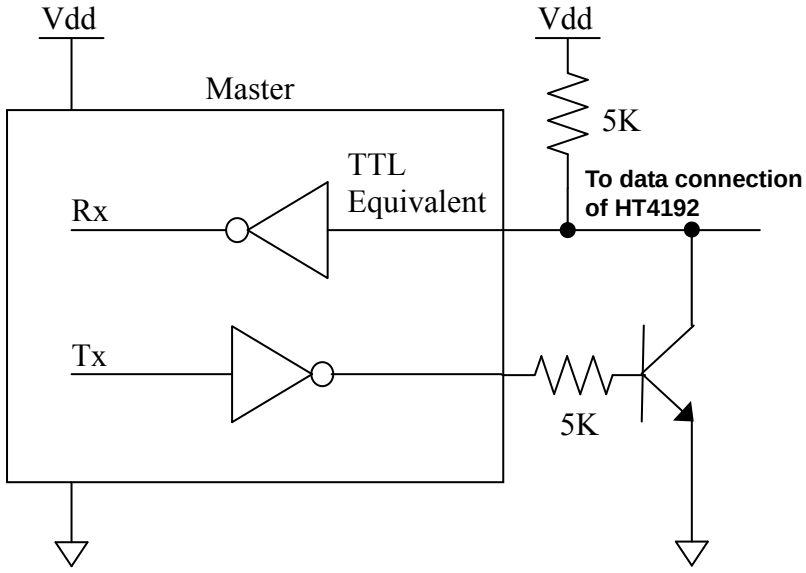


**BUS MASTER CIRCUIT** Figure 3

(A) Open Drain




(B) Standard TTL




Note:
Depending on the HT-Wire communication speed and the bus load characteristics,the optimal pullup Resistor ($R_{PU}$) value will be in the 1.5kΩ to 5kΩ range.

## TRANSACTION SEQUENCE

The sequence for accessing the HT4192 via the HT-Wire port is as follows:

※ Initialization
※ ROM Function Command
※ Read Data

## INITIALIZATION

All transactions on the HT-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a Presence Pulse(s) transmitted by the slave(s).The Presence Pulse lets the bus master know that the HT4192 is on the bus and is ready to operate.

## ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are 8 bits long. A list of these commands follows (refer to flowchart in Figure4).

## Read ROM [33h] or [0Fh]

This command allows the bus master to read the HT4192's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single HT4192 on the bus. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The HT4192 Read ROM function will occur with a command byte of either 33h or 0Fh in order to ensure compatibility with the Dallas Series.

## HT-Wire SIGNALING

The HT4192 requires a strict protocol to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with Reset Pulse and Presence Pulse, write 0, write 1, and read data. All these signals except Presence Pulse are initiated by the bus master.

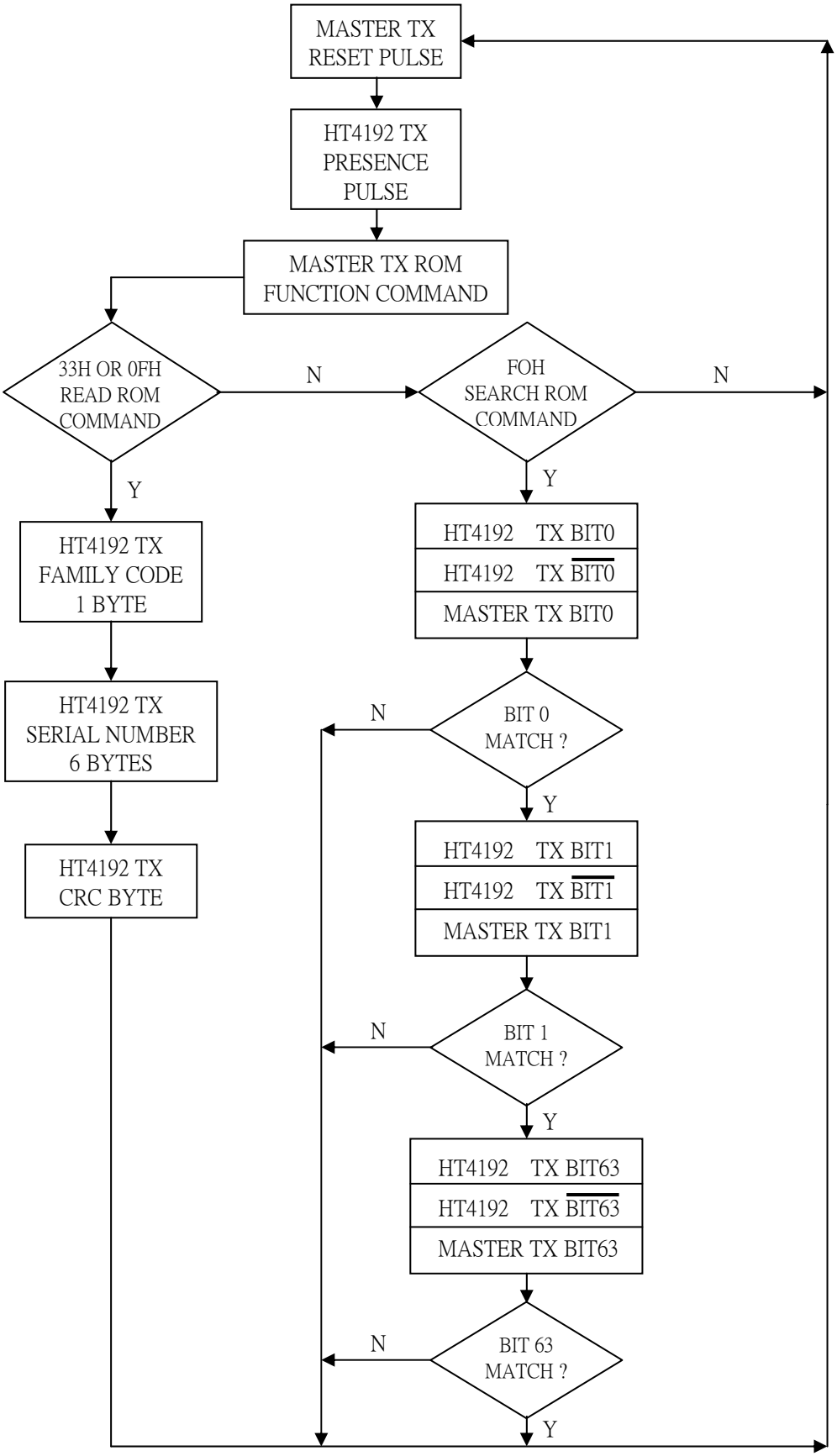
The initialization sequence required to begin any communication with the HT4192 is shown in Figure 5.A reset pulse followed by a Presence Pulse indicates the HT4192 is ready to send or receive data giventhe correct ROM command.

The bus master transmits (TX ) a reset pulse (tRSTL , minimum 480 $\mu$s). The bus master then releases the line and goes into receive mode (RX ). The HT-Wire bus is pulled to a high state via the 5kΩ pullup resistor.After detecting the rising edge on the data pin, the HT4192 waits (tPDH, 15-60 $\mu$s) and then transmits the Presence Pulse (tPDL, 60-240 $\mu$s). The HT-Wire bus requires a pullup resistor range of 1.5kΩ to 5kΩ,depending on bus load characteristics.

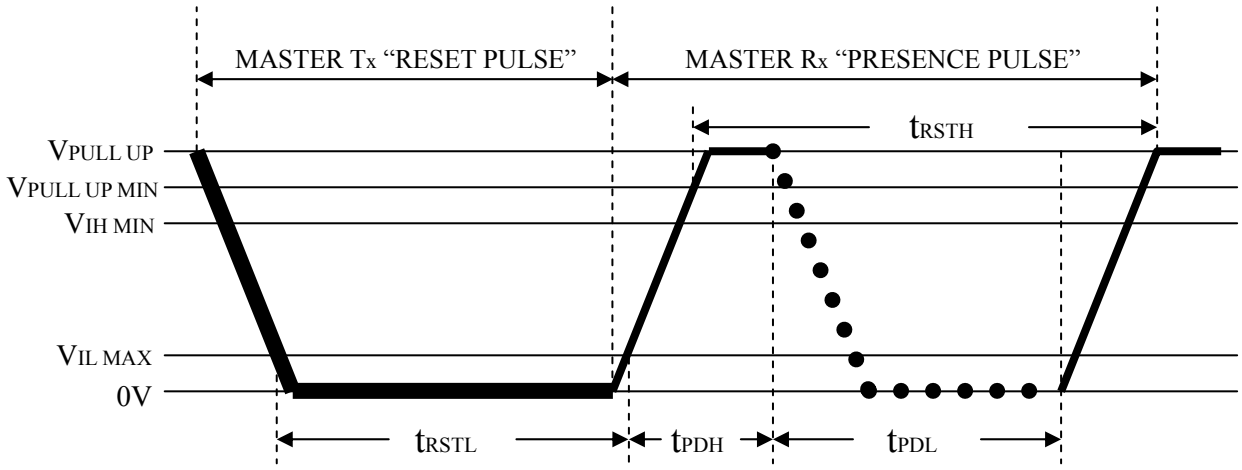
## READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 6. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the HT4192 to the master by triggering a delay circuit in the HT4192. During write time slots, the delay circuit determines when the HT4192 will sample the data line. For a read data time slot, if a "0" is to be transmitted, the delay circuit determines how long the HT4192 will hold the data line low overriding the "1" generated by the master.If the data bit is a 1, the HT4192 will leave the read data time slot unchanged.

**FUNCTIONS FLOW CHART Figure 4**

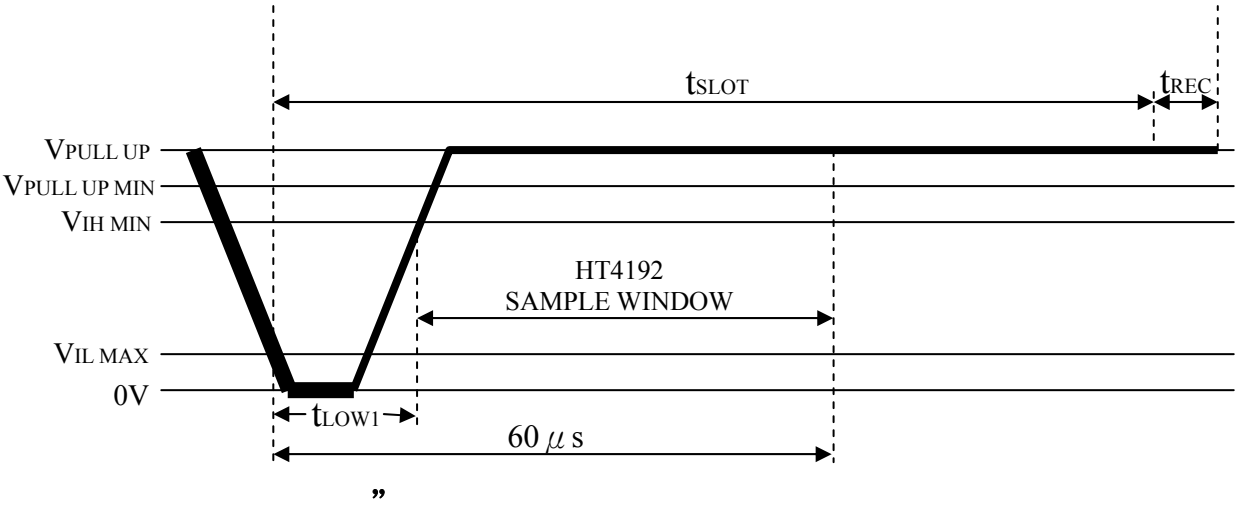


**INITIALIZATION PROCEDURE "RESET AND PRESENCE PULSES" Figure 5**

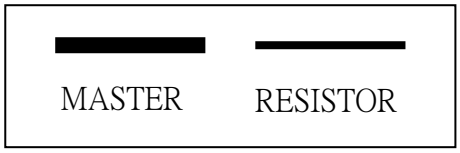



* In order not to mask interrupt signaling by other devices on the HT-Wire bus, $t_{RSTL} + t_R$ should always be less than 960 $\mu$s.

**READ/WRITE TIMING DIAGRAM Figure 6**
**Write-One Time Slot**

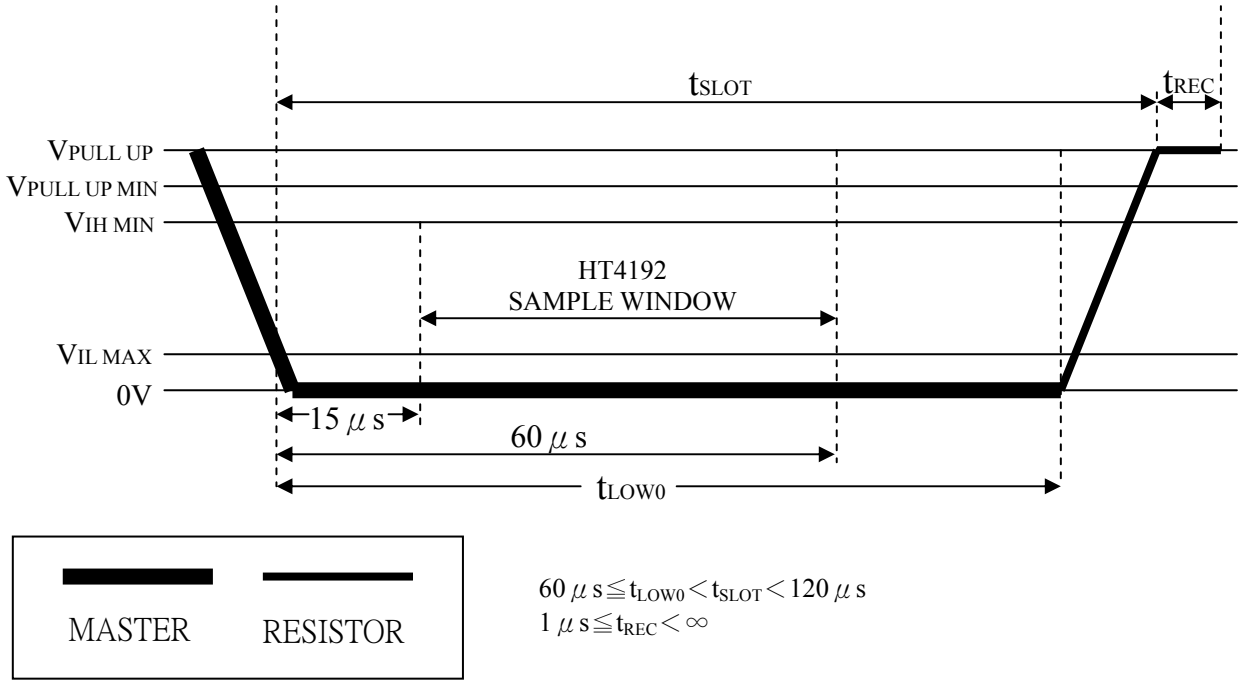



"



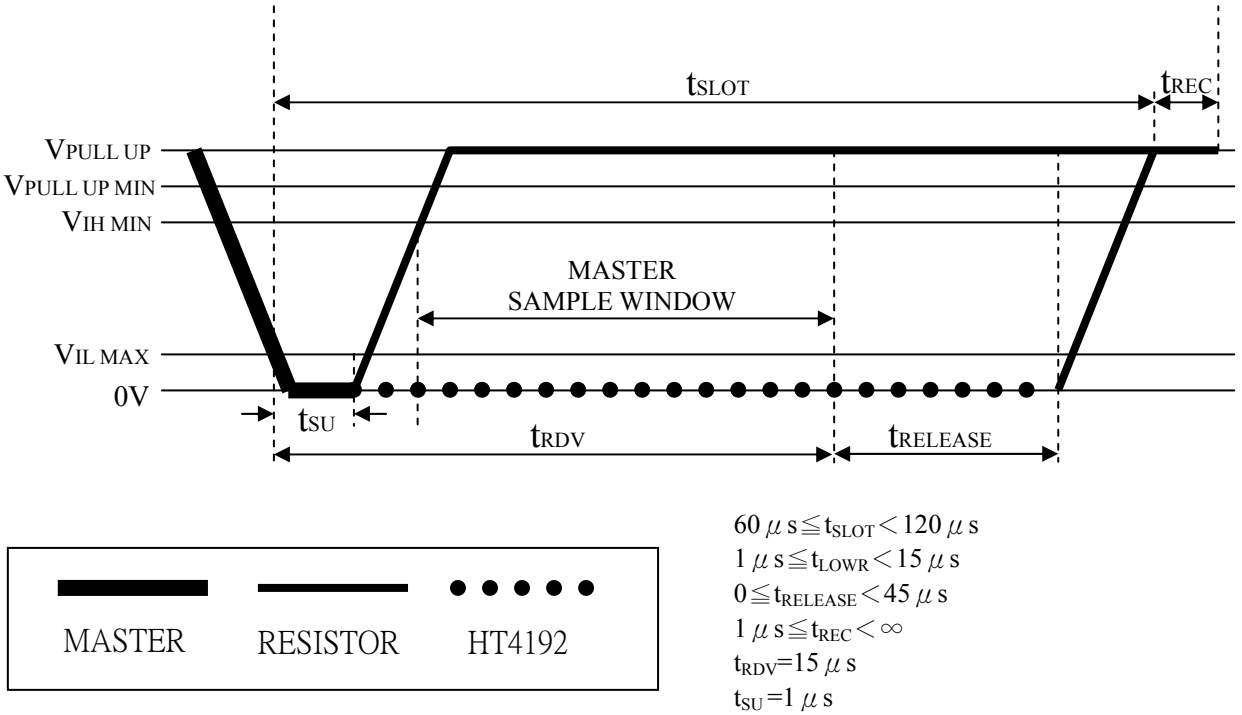

$60\ \mu s \leqq t_{SLOT} < 120\ \mu s$
$1\ \mu s \leqq t_{LOW1} < 15\ \mu s$
$1\ \mu s \leqq t_{REC} < \infty$

**READ/WRITE TIMING DIAGRAM (cont'd) Figure 6**
**Write-Zero Time Slot**




$60\,\mu s \leqq t_{LOW0} < t_{SLOT} < 120\,\mu s$
$1\,\mu s \leqq t_{REC} < \infty$

**Read-data Time Slot**




$60\,\mu s \leqq t_{SLOT} < 120\,\mu s$
$1\,\mu s \leqq t_{LOWR} < 15\,\mu s$
$0 \leqq t_{RELEASE} < 45\,\mu s$
$1\,\mu s \leqq t_{REC} < \infty$
$t_{RDV} = 15\,\mu s$
$t_{SU} = 1\,\mu s$

## CRC GENERATION

To validate the data transmitted from the HT4192, the bus master may generate a CRC value from the data as it is received. This generated value is compared to the value stored in the last 8 bits of the HT4192. If the two CRC values match, the transmission is error-free.
The equivalent polynomial function of this CRC is: CRC = x8 + x5 + x4 + 1.

## CUSTOM HT4192

Customization of a portion of the unique 48-bit serial number by the customer is available. HHTC CORP. will register and assign a specific customer ID in the 12 most significant bits of the 48-bit field. The next most significant bits are selectable by the customer as a starting value, and the least significant bits are non-selectable and will be automatically incremented by one. Certain quantities and conditions apply for these custom parts. Contact your HHTC CORP sales representative for moreinformation.

## CHIP DIMENSIONS