HT51469DS RFID Card Reader

HT51469DS is a RFID read module（13.56MHz），this is only for HT4169 reading，the output format is base on Wiegand 26、Wiegand 34、DS1990 and reading data will output from DATA0 and DATA1。

A、Product spec：

Type	HT51469DS
Output format	Wiegand 26、Wiegand 34、DS1990
Size	26(Diameter)×22(Height)m/m
Operation frequency	13.56MHz

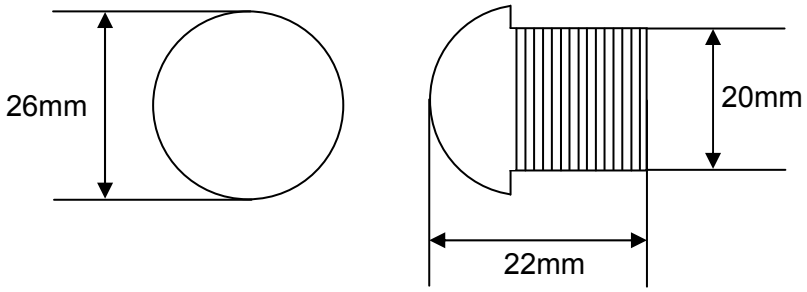
HT51469DS X

A：Wiegand 26
B：Wiegand 34
C：DS1990

B、Technology parameter：

Operation voltage	VCC=8~18V
Consumption current	60mA
I/O output current	25mA sink/source
Operation temperature	- 40℃ ～ + 85℃
Storage temperature	- 40℃ ～ + 85℃
Storage humidity	5 ～ 95% RH

C、Dimension of module：



D、Pin assignment and electronic parameter：

1.Wiegand 26 & Wiegand 34

PIN	NAME	I/O	SYMBLE	MIN	TYP	MAX	DESCRIPTION
1	VCC(Red)	I		8V	-	18V	VCC
2	GND(Black)	I		-		-	Digital Ground
3	LED(Yellow)	I	Vi-H Vi-L	Vcc-0.2V -	Vcc GND	Vcc+0.2V Vss+0.2V	Open :LED ON Low:LED OFF
4	DATA1(Green)	O	Vo-H Vo-L	5V-0.2V -	5V GND	5V+0.2V GND+0.2V	Digital data output
5	DATA0(White)	O	Vo-H Vo-L	5V-0.2V -	5V GND	5V+0.2V GND+0.2V	Digital data output

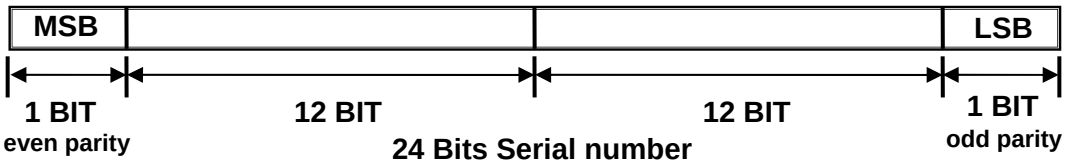
2.DS1990

PIN	NAME	I/O	SYMBLE	MIN	TYP	MAX	DESCRIPTION
1	VCC(Red)	I		8V	-	18V	VCC
2	GND(Black)	I		-		-	Digital Ground
3	LED(Yellow)	I	Vi-H Vi-L	Vcc-0.2V -	Vcc GND	Vcc+0.2V Vss+0.2V	Open :LED ON Low:LED OFF
4	DATA1(Green)	O	Vo-H Vo-L	5V-0.2V -	5V GND	5V+0.2V GND+0.2V	Digital data output
5	DATA0(White)	I	-	-	-	-	Connect GND

E、Wiegand code

1.Format of data output

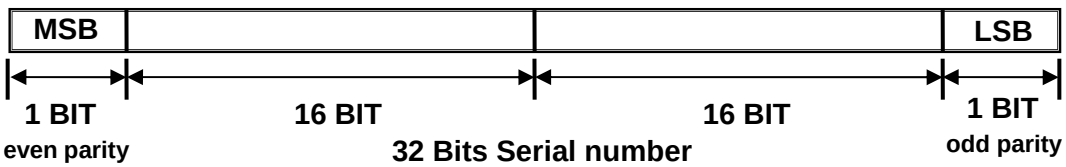
a.Wiegand 26



※ **MSB will be send first.**

※ **MSB's 12 Bits is base on even parity，LSB's 12Bits is base on odd parity.**

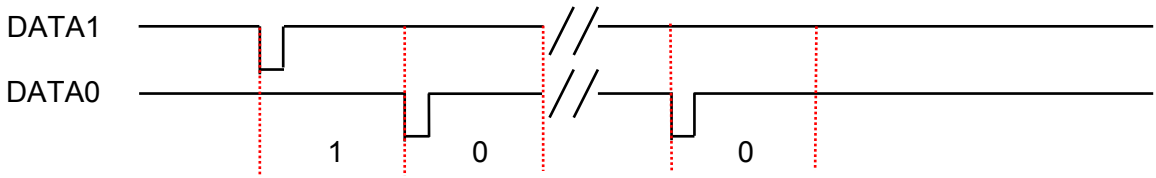
b.Wiegand 34

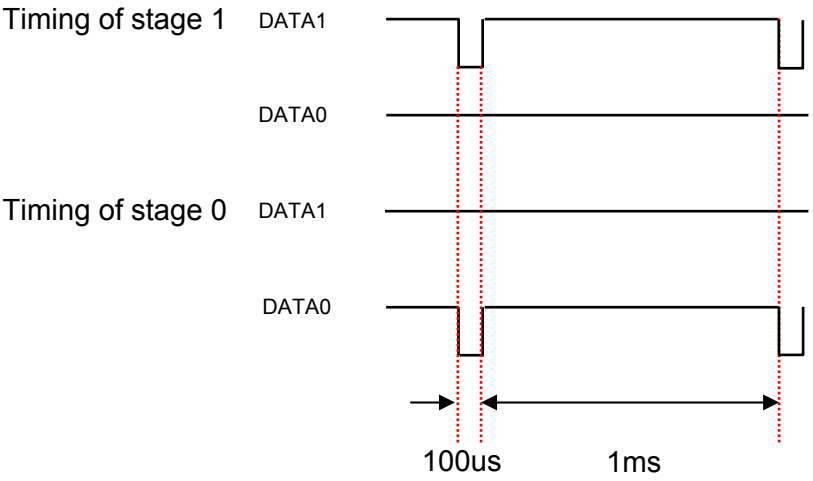


※ **MSB will be send first.**

※ **MSB's 12 Bits is base on even parity，LSB's 12Bits is base on odd parity.**

2.Timing sequence





F、DS1990 format

1. Format of data output

8-Bit CRC Code		48-Bit Serial Number		8-Bit Family Code	
MSB	LSB	MSB	LSB	MSB	LSB

※ MSB will be send first.

a.INITIALIZATION

All transactions on the 1 bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by a Presence Pulse(s) transmitted by the slave(s).The Presence Pulse lets the bus master know that the HT51469DS is on the bus and is ready to operate.

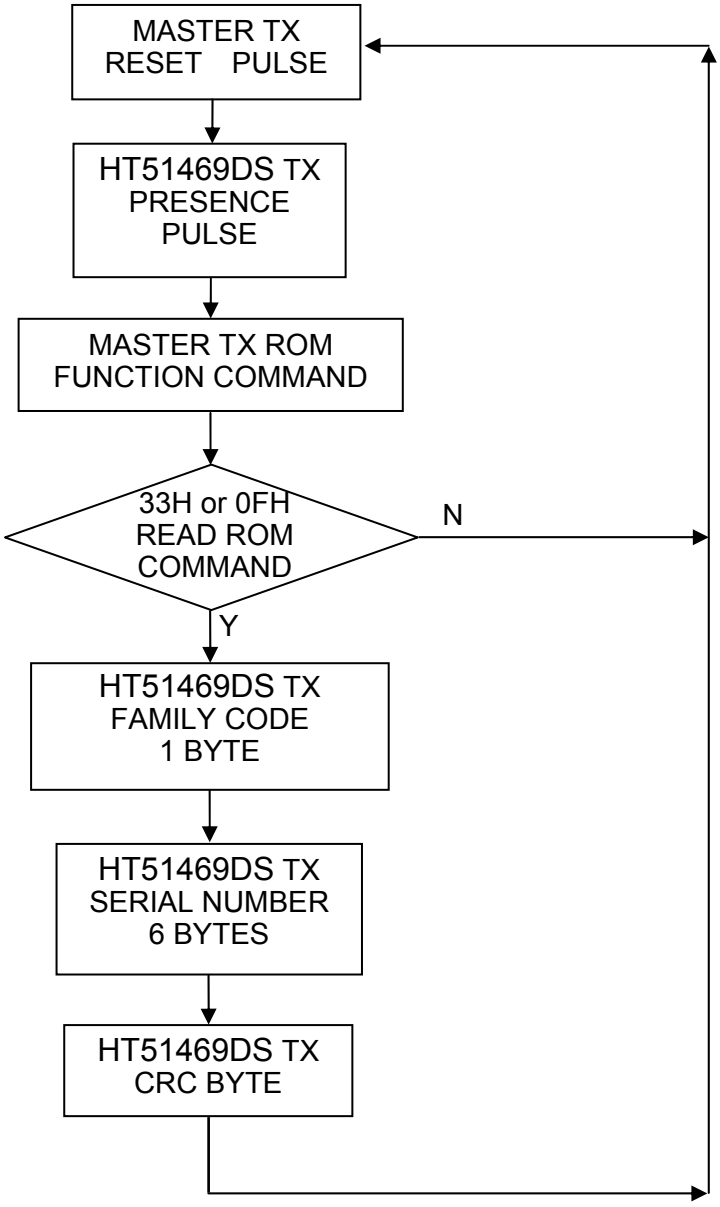
b.ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the four ROM function commands. All ROM function commands are 8 bits long. A list of these commands follows (refer to flowchart in Figure1).

c.Read ROM [33H] or [0FH]

This command allows the bus master to read the HT51469DS's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. If more than one slave is present on the bus, a data collision will occur when all slaves try to transmit at the same time (open drain will produce a wired-AND result). The HT51469DS Read ROM function will occur with a command byte of either 33h or 0Fh in order to ensure compatibility.

d.ROM FUNCTIONS FLOW CHART (Figure 1)



2.Timing sequence

The HT51469DS requires a strict protocol to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with Reset Pulse and Presence Pulse, write 0, write 1, and read data. All these signals except Presence Pulse are initiated by the bus master.

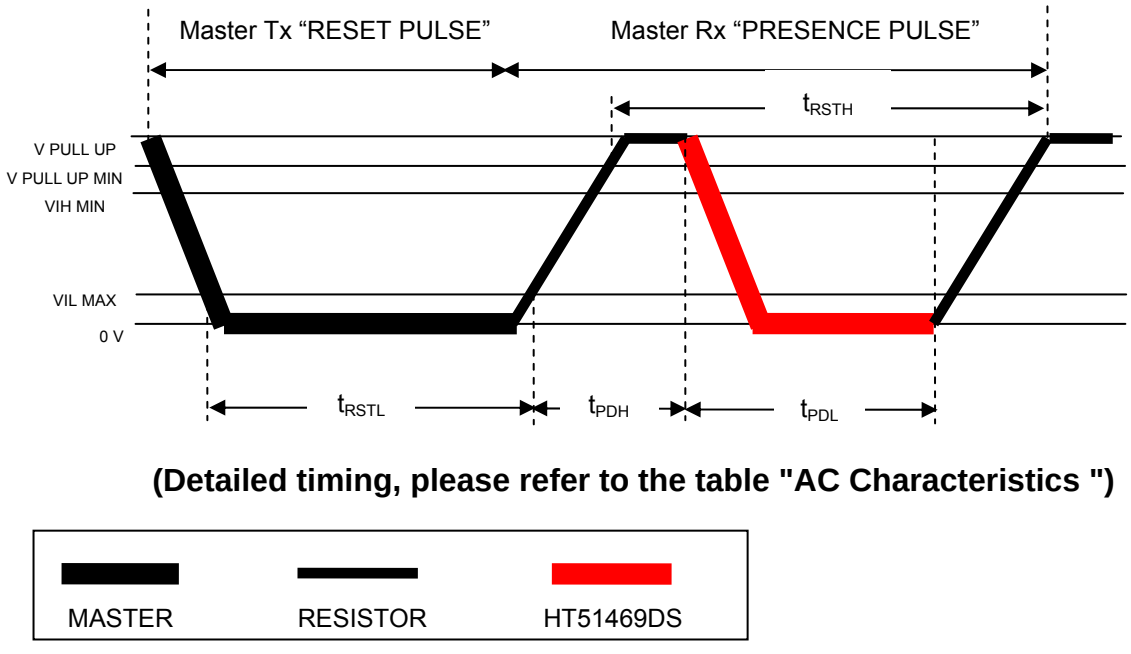
The initialization sequence required to begin any communication with the HT51469DS is shown in Figure 2.A reset pulse followed by a Presence Pulse indicates the HT51469DS is ready to send or receive data given the correct ROM command.

The bus master transmits (TX) a reset pulse (t_{RSTL} , minimum 480μs). The bus master then releases the line and goes into receive mode (RX). The bus is pulled to a high state via the 5kΩ pullup resistor.After detecting the rising edge on the data pin, the HT51469DS waits (t_{PDH}, 15-60μs) and then transmits the Presence Pulse (t_{PDL}, 60-240μs). The bus requires a pullup resistor range of 1.5kΩ to 5kΩ,depending on bus load characteristics.

a.READ/WRITE TIME SLOTS

The definitions of write and read time slots are illustrated in Figure 3. All time slots are initiated by the master driving the data line low. The falling edge of the data line synchronizes the HT51469DS to the master by triggering a delay circuit in the HT51469DS. During write time slots, the delay circuit determines when the HT51469DS will sample the data line. For a read data time slot, if a “0” is to be transmitted, the delay circuit determines how long the HT51469DS will hold the data line low overriding the “1” generated by the master.If the data bit is a 1, the HT51469DS will leave the read data time slot unchanged.

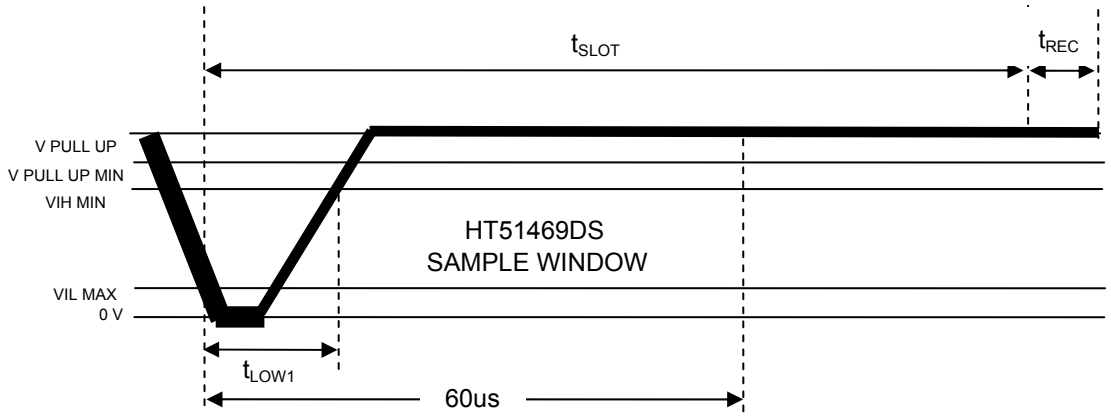
INITIALIZATION PROCEDURE” RESET AND PRESENCE PULSES” Figure2



(Detailed timing, please refer to the table "AC Characteristics ")

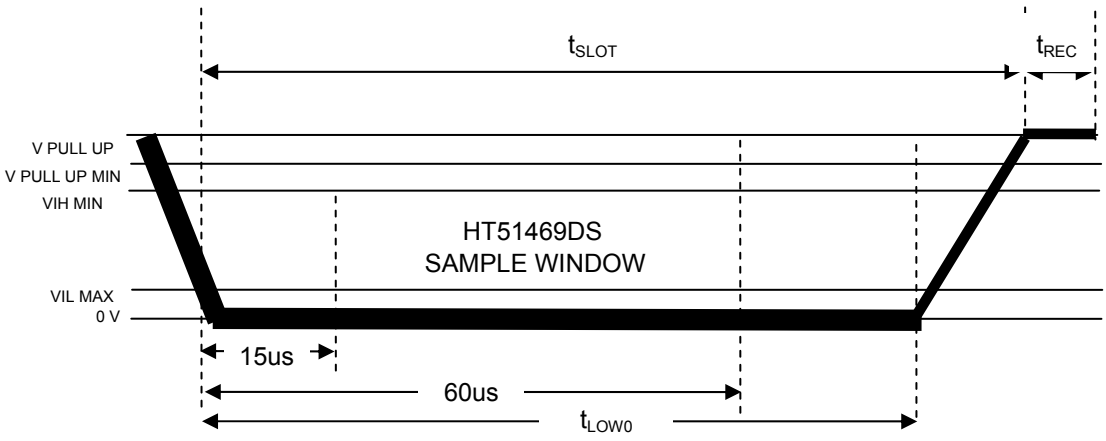
READ/WRITE TIME SLOTS (Figure 3)

Write-One Time Slot



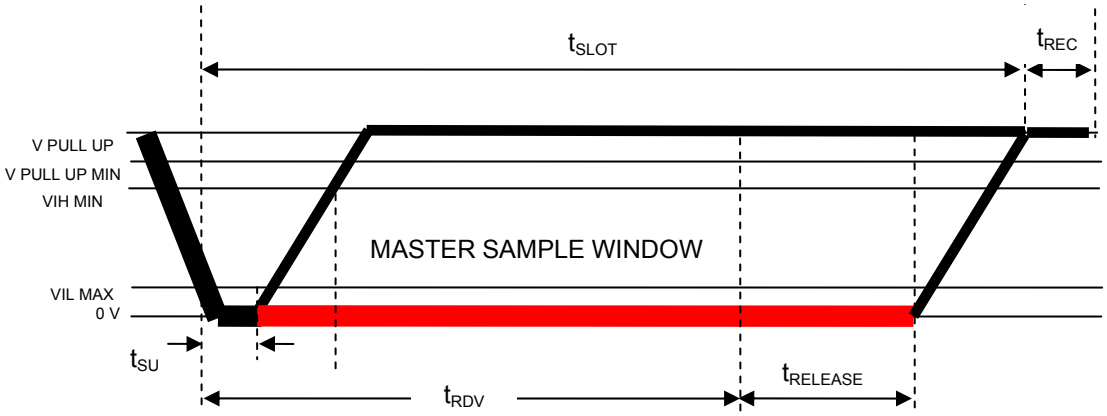
(Detailed timing, please refer to the table "AC Characteristics ")

Write-Zero Time Slot



(Detailed timing, please refer to the table "AC Characteristics ")

Read-data Time Slot



(Detailed timing, please refer to the table "AC Characteristics ")

b.CRC GENERATION

To validate the data transmitted from the HT51469DS, the bus master may generate a CRC value from the data as it is received. This generated value is compared to the value stored in the last 8 bits of the HT51469DS. If the two CRC values match, the transmission is error-free.The equivalent polynomial function of this CRC is:

$$CRC = X^8 + X^5 + X^4 + 1$$

c.AC Characteristics (V_{PUP} = 2.8V ～ 6.0V ； -40°C ～ +85°C)

Parameters	SYMBLE	MIN	TYP	MAX	Unit
Slot	t_{SLOT}	60		120	μs
Write 1 low Level Time	t_{LOW1}	1		15	μs
Write 0 low Level Time	t_{LOW0}	60		120	μs
Read data valid	t_{RDV}	15 (Exact value)			μs
Release time	$t_{RELEASE}$	0	15	45	μs
Read data setup time	t_{SU}			1	μs
Recovery time	t_{REC}	1			μs
Reset Time High Level	t_{RSTH}	480			μs
Reset Low Level Time	t_{RSTL}	480			μs
Online High Level Detection	t_{PDH}	15		60	μs
Online Low Level Detection	t_{PDL}	60		200	μs